Syllabus of Spring Semester, 2018

Course Title	Digital Integrated Circuits	Course Code	EB68683	Section	001
Department	Electronics Engineering	Level	All	Credit - Theory - Practice	3.0 - 3.0 - 0.0
Class Hours & Classroom	Thu. 14:00-17:00 108-9401				
Lecturer	KIM,JAE-HO	Office	기전관 408	Office Hours	Mon 3:00-5:00 PM
		Telephone	010-4042-2450	E-mail	jhkim@pusan.ac.kr
Methodology of Instruction	Lecture and Coding				
Evaluation and Grading	Homework - 30% Mid and Final Exam 60% Attend and others 10% * Students with disabilities can request an extension of the exam hour, and they can take exams by getting writing assistance or by using a computer.				
Prerequisites	Logic Design or Equvalent lectures				
Course Objectives	Developing Logic System Design Capability using VHDL				
Course Description	1. Digital Watch Design 2. VHDL is 3. Entity and Architecture 4. Designing Simple Combinational Circuits 1 5. Designing Simple Combinational Circuits 2 6. Hierachical Design and Process 7. Mid Term Exam 8. Designing Sequential Circuits 9. Finite State Machine 10. Behavioral and Structual Design 11. Digital Watch in VHDL 12. CPU and VHDL 1 13. CPU and VHDL 2 14. Memory and IO 15. Final Exam * Students with disabilities can negotiate with the Disabled Student's Academic Support Center regarding course materials and assignments.				
Textbooks and References					
Required Textbooks					
References					

Weekly Schedule of Classes		
Week No.	Course Material	Assignments and Other Notes
Week 1	[Orientation and Education on Academic Misbehavior(e.g. Cheating, Plagiarism) and Safety Education on Experiment and Practice] Digital Watch Design	Analysis of Digital Watch Design
Week 2	VHDL is	
Week 3	Entity and Architecture	
Week 4	Designing Simple Combinational Circuits 1	
Week 5	Designing Simple Combinational Circuits 2	Design and Verification of the componots of Digital Watch
Week 6	Hierarchical Design and Process	
Week 7	Mid Term Exam	
Week 8	Designing Sequential Circuits	
Week 9	Finite State Machine	
Week10	Behavioral and Structural Design	
Week11	Digital Watch in VHDL	Completing Digital Watch
Week12	CPU and VHDL 1	
Week13	CPU and VHDL 2	Design and Verfication of the components of CPU
Week14	Memory and IO	Verifying CPU Operation
Week15	Final Exam	
Week16		
Attachment		